Claims:

1. A method for storing macroblocks in a memory, said method comprising:

decoding a macroblock; and

executing an instruction, wherein the instruction causes:

writing the macroblock to the memory.

2. The method of claim 1, wherein writing the macroblock to the memory further comprises:

writing a luminance matrix to a first portion of the memory;

writing a first chrominance matrix to second portion of the memory;

writing a second chrominance matrix to a third portion of the memory; and

the first portion, second portion, and third portion being contiguous.

3. A method for storing macroblocks in a memory, said method comprising:

decoding five macroblocks; and

executing an instruction, wherein the instruction causes:

writing the five macroblocks to the memory.

4. The method of claim 3, wherein writing the five macroblock to the memory further comprises:

writing five luminance matrices to a first five portions of the memory;

writing five chrominance matrix to a second five portions of the memory;

writing five chrominance matrix to a third five portions of the memory; and

the first five portions, second five portions, and third five portions being contiguous.

5. A circuit for storing macroblocks, said circuit comprising:

a decoder for decoding macroblocks; and

a computer readable medium storing an executable instruction, wherein the instruction causes:

writing the macroblock to the memory.

6. The circuit of claim 5, wherein writing the macroblock to the memory further comprises:

writing a luminance matrix to a first portion of the memory;

writing a first chrominance matrix to second portion of the memory;

writing a second chrominance matrix to a third portion of the memory; and

the first portion, second portion, and third portion being contiguous.

7. A circuit for storing macroblocks, said circuit comprising:

a decoder for decoding five macroblocks; and

a computer readable medium storing an executable instruction, wherein the instruction causes:

writing the five macroblocks to the memory.

8. The circuit of claim 7, wherein writing the five macroblock to the memory further comprises:

writing five luminance matrices to a first five portions of the memory;

writing five chrominance matrix to a second five portions of the memory;

writing five chrominance matrix to a third five portions of the memory; and

the first five portions, second five portions, and third five portions being contiguous.